//testbench

module testbench;

reg t, clk;

wire q, qb;

tflipflop uut(.t(t), .clk(clk), .q(q), .qb(qb));

initial begin

clk = 0;

forever #5 clk = ~clk;

end

initial begin

$dumpfile("tflipflop.vcd");

$dumpvars(1);

end

initial begin

t=0;

#5;

t=1;

#5;

t=1;

#10;

t=0;

#10;

t=1;

#10;

$finish;

end

endmodule

//design

module tflipflop(t, clk, reset, q,qb);

input t, clk, reset;

output q,qb;

reg q; wire qb;

initial q=0;

always @(posedge clk or posedge reset)

begin

if (reset)

q <= 0;

else

q = (t == 1) ? ~q : q;

end

assign qb = ~q;

endmodule